

Timers

- Timer 0,1,2
- 8 bits or 16 bits
- Clock sources:
 - □ Internal clock,
 - □ Internal clock with prescaler,
 - □ External clock (timer 2),
 - □ Special input pin

Features

- The choice of timers clock frequency (prescaler)
- Read / write counter status
- Waveform generation using a comparison register
- Frequency adjustment, PWM (Pulse Width Modulation)
- Interrupt request generation at regular intervals
- Triggered by an external event (capture)

Usage

- Wave generation
- Accurate program execution timing (event management),
- Signal timing measurement

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Configuration

Bit	7	6	5	4	3	2	1	0	_
	FOC0	WGM00	COM01	COM00	WGM01	CS02	CS01	CS00	TCCR0
Read/Write	W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	-
Initial Value	0	0	0	0	0	0	0	0	

- Register TCCRn controls the timer behavior
 - □ FOC0: Force Output Compare
 - □ WGM0[1:0]: Waveform Generation Mode
 - □ COM01:0: Compare Match Output Mode
 - □ CS02:0: Clock Select



0.501	C500	Description
0	0	No clock source (Timer/Counter stopped).
0	1	clk _{I/O} /(No prescaling)
1	0	clk _{I/O} /8 (From prescaler)
1	1	clk _{I/O} /64 (From prescaler)
0	0	clk _{I/O} /256 (From prescaler)
0	1	clk _{I/O} /1024 (From prescaler)
1	0	External clock source on T0 pin. Clock on falling edge.
1	1	External clock source on T0 pin. Clock on rising edge.
	0 0 1 1 0 0 1 1 1	CSU1 CSU2 0 0 0 1 1 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 1 0 1 1 1 1

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8-bit Timer/Counter Block Diagram



Counter Unit



- count Increment or decrement TCNT0 by 1.
- direction Select between increment and decrement
- clear Clear TCNT0

- **clk**_{Tn} Timer/Counter clock
- TOP Signalize that TCNT0 has reached maximum value
- BOTTOM Signalize that TCNT0 has reached minimum value (zero).

Output Compare Unit



Output Compare Unit



			1	Normal, CI	
			//	COM0[1:0]	Description
Μ	odes d	of Operation		00	Normal, OC0 disconnected.
		•		01	Toggle OC0 on compare match
				10	Clear OC0 on compare match
				11	Set OC0 on compare match
ode	WGM01:00	Mode	// .	PWM. Phase	e Correct
0	00	Normal		COM0[1:0]	Description
1	01	PWM, Phase Correct	T	00	Normal. OC0 disconnected.
2	10	CTC		01	Reserved
				01	INCOCIVED
3	11	Fast PWM	\	01	Clear OC0 on compare match wh
3	11	Fast PWM	\backslash	10	Clear OC0 on compare match wh up-counting. Set OC0 on compare
3	11	Fast PWM	\backslash	10	Clear OC0 on compare match wh up-counting. Set OC0 on compare match when downcounting
³ The	¹¹ mode of	Fast PWM		10	Clear OC0 on compare match wh up-counting. Set OC0 on compare match when downcounting Set OC0 on compare match when
3 The defii	ned by the	Fast PWM operation is e combination of		10 11	Clear OC0 on compare match wh up-counting. Set OC0 on compare match when downcounting Set OC0 on compare match wher up-counting. Clear OC0 oncompa
³ The defin the	node of mode of mode of which we have been stated by the Waveform	Fast PWM operation is e combination of n Generation		10 11 Fast PWM	Clear OC0 on compare match wh up-counting. Set OC0 on compare match when downcounting Set OC0 on compare match wher up-counting. Clear OC0 oncompa match when downcounting
3 The defin the	node of med by the Waveform	Fast PWM operation is e combination of n Generation 01:0) and		10 11 Fast PWM COM0[1:0]	Clear OC0 on compare match wh up-counting. Set OC0 on compare match when downcounting Set OC0 on compare match wher up-counting. Clear OC0 oncompa match when downcounting Description
³ he lefii he Con	node of ned by the Waveform de (WGM0 npare Out	Fast PWM operation is e combination of n Generation 01:0) and put mode		10 11 Fast PWM COM0[1:0] 00	Clear OC0 on compare match wh up-counting. Set OC0 on compare match when downcounting Set OC0 on compare match wher up-counting. Clear OC0 oncompa match when downcounting Description Normal, OC0 disconnected.
3 The defin the the Con	11 mode of a ned by the Waveform de (WGM0 npare Out M01:0) bi	Fast PWM operation is e combination of n Generation 01:0) and put mode ts		10 11 Fast PWM COM0[1:0] 00 01	Clear OC0 on compare match wh up-counting. Set OC0 on compare match when downcounting Set OC0 on compare match wher up-counting. Clear OC0 oncompa match when downcounting Description Normal, OC0 disconnected. Reserved
³ lefin he ¹ noc Con	11 mode of o ned by the Waveform de (WGMC npare Out M01:0) bi	Fast PWM operation is e combination of n Generation 01:0) and put mode ts		10 11 Fast PWM COM0[1:0] 00 01	Clear OC0 on compare match wh up-counting. Set OC0 on compare match when downcounting Set OC0 on compare match wher up-counting. Clear OC0 oncompa match when downcounting Description Normal, OC0 disconnected. Reserved Clear OC0 on compare match, se
3 The defin the Con (CO	11 mode of of med by the Waveform de (WGM0 mpare Out M01:0) bi	Fast PWM operation is e combination of n Generation 01:0) and put mode ts		10 11 Fast PWM COM0[1:0] 00 01 10	Clear OC0 on compare match wh up-counting. Set OC0 on compare match when downcounting Set OC0 on compare match wher up-counting. Clear OC0 oncompa match when downcounting Description Normal, OC0 disconnected. Reserved Clear OC0 on compare match, se OC0 at BOTTOM
3 Jefii he V noc CO	11 mode of a med by the Waveform de (WGM0 mpare Out M01:0) bi	Fast PWM operation is combination of Generation 01:0) and put mode ts		10 11 Fast PWM COM0[1:0] 00 01 10	Clear OC0 on compare match wh up-counting. Set OC0 on compare match when downcounting Set OC0 on compare match when up-counting. Clear OC0 oncompare match when downcounting Description Normal, OC0 disconnected. Reserved Clear OC0 on compare match, set OC0 at BOTTOM Set OC0 on compare match, clear

Modes of Operation

Normal Mode

- □ The counting direction is always up (incrementing)
 - 8 bits (Timer 0,2) between 0 to 255
 - 16 bits (Timer 1) between 0 to 65535
- The counter simply overruns when it passes its maximum value and then restarts from the bottom.
 - Timer overflow interrupt appears

Modes of Operation



CTC – Clear Timer on Compare Match

Example:

- Timer1 in CTC mode (Clear Timer on Compare Match)
 - $\hfill\square$ the selected clock source increments the timer
 - \Box the current value is held in TCNT1 (starts at 0)
 - when TCNT1 = OCRA1, an interrupt is issued and the timer is reset
 - □ by choosing OCR1A and the clock frequency, the timer can be programmed for any time interval

					7	6	5	4	3	2	1	0	
				co	M1A1 COM	11A 0	COM1B1	COM1B0	FOC1A	FOC1B	WGM11	WGM10	TCCR1A
Т	'ime	r1 reg	qister	′s ¯	R/W R	W	R/W	R/W	W	W	R/W	R/W	-
				_	7 6		5	4	3	2	1	0	
				IC	NC1 ICE	S1	-	WGM13	WGM12	CS12	CS11	CS10	TCCR1B
				F	R/W R/	W	R	R/W	R/W	R/W	R/W	R/W	
	Mode	WGM13	WGM12 (CTC1)	WGM11 (PWM11)	WGM10 (PWM10)	Tim	er/Counter	r Mode of Op	peration	тор	Update of OCR1X	TOV1 F on	lag Set
	0	0	0	0	0	Nor	mal			0xFFFF	Immediate	MAX	
	1	0	0	0	1	PW	M, Phase C	orrect, 8-bit		0x00FF	TOP	BOTTO	M
	2	0	0	1	0	PW	M, Phase C	orrect, 9-bit		0x01FF	ТОР	BOTTO	M
	3	0	0	1	1	PW	M, Phase C	orrect, 10-bi	t	0x03FF	ТОР	BOTTO	M
C	4	0	1	0	0	СТС)			OCR1A	Immediate	MAX	
	5	0	1	0	1	Fast	t PWM, 8-b	it		0x00FF	BOTTOM	TOP	
	6	0	1	1	0	Fast	t PWM, 9-b	it		0x01FF	BOTTOM	TOP	
	7	0	1	1	1	Fast	t PWM, 10-	bit		0x03FF	BOTTOM	TOP	
	8	1	0	0	0	PWI	M, Phase a	nd Frequenc	y Correct	ICR1	BOTTOM	BOTTO	M
	9	1	0	0	1	PWI	M, Phase a	nd Frequenc	y Correct	OCR1A	BOTTOM	BOTTO	М
	10	1	0	1	0	PW	M, Phase C	Correct		ICR1	ТОР	BOTTO	M
	11	1	0	1	1	PW	M, Phase C	orrect		OCR1A	TOP	BOTTO	M
	12	1	1	0	0	СТС)			ICR1	Immediate	MAX	
	13	1	1	0	1	Res	erved			-	-	-	
	14	1	1	1	0	Fast	PWM			ICR1	BOTTOM	TOP	
	15	1	1	1	1	Fast	PWM			OCR1A	BOTTOM	TOP	

Prescaler clock division



CS02	CS01	CS00	Description
0	0	0	No clock source (Timer/Counter stopped).
0	0	1	clk _{I/O} /(No prescaling)
0	1	0	clk _{I/O} /8 (From prescaler)
0	1	1	clk _{I/O} /64 (From prescaler)
1	0	0	clk _{I/O} /256 (From prescaler)
1	0	1	clk _{I/O} /1024 (From prescaler)
1	1	0	External clock source on T0 pin. Clock on falling edge.
1	1	1	External clock source on T0 pin. Clock on rising edge.

Example:

- Timer 1 intrerrupt generated each 1s
 - \Box 1 s => low frequency
 - □ f_{cuart} =13.5MHz→division by 13,500,000 > 65536 (16 bits) → impossible
 - $\hfill\square$ we need the prescaler to divide some more
 - □ prescaler: max divisor = 1024; 13.5MHz / 1024 = 13.184 kHz
 - \Box we want 1Hz: we div ide again by 13184 = 3380h
 - □ OCR1AH = 33h, OCR1AL = 80h
 - □ we select the CTC mode; let's set the remaining registers
 - \Box from the 2 previous tables: TCCR1A = 0 and
 - □ TCCR1B= 00001101 = 0Dh

Good News !

- All these calculations can be done using CodeWizard
- You still need to read the datasheet for the explanation of the different modes



Modes of Operation

Fast PWM mode

useful for setting the speed of a motor or the light intensity of a light source



□ The mean value can be within maximum and minimum values, depending on *D*

$$V_{MED} = DV_{CC} + (1 - D)V_{GND}$$

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Fast PWM mode

- □ Frequency is fixed by the clock select bits CSn2:0
- □ Duty factor is set by writing OCR0 register





Fast PWM mode

Example: How to calculate the PWM frequency Use the timer/counter0 in PWM mode

Bit	7	6	5	4	3	2	1	0	
]	FOC0	WGM00	CON	01 COM00	WGM01	CS02	CS01	CS00	TCCR0
Read/Write	W	R/W	R/V	V R/W	R/W	R/W	R/W	R/W	•
Initial Value	0	0	0	0	0	0	0	0	
	CS02	CS01	CS00	Description					
	0	0	0	No clock source (1	Fimer/Counter	stopped).			
	0	0	1	clk _{i/O} /(No prescali	ing)				
	0	1	0	clk _{I/O} /8 (From pres	scaler)				
	0	1	1	clk _{I/O} /64 (From pr	escaler)				
	1	0	0	clk _{I/O} /256 (From p	rescaler)				
	1	0	1	clk _{I/O} /1024 (From	prescaler)				
	1	1	0	External clock sou	irce on T0 pin.	Clock on fallin	g edge.		
	1	1	1	External clock sou	irce on T0 pin.	Clock on risin	g edge.		21

How to calculate the PWM frequency

- PWM \rightarrow the frequency is constant, the duty cycle varies
- Assume f_{crystal} = 13.5MHz, we divide it by:
 - □ prescaler: max 1024
 - □ maximum value for the 8 bit timer register: 256
 - \square we have f_{PWM} = 13500000/1024/256 = 51 Hz
 - Note: 51Hz is enough for light bulbs or motors, but a 51Hz flicker is visible on LEDs
 - □ we choose a lower prescaler: 256
 - □ f_{PWM} = 13500000/256/256 = 205 Hz
 - □ Prescaler=256 \rightarrow CS02:00 = 100 (see previous table)

e a								Time	r/C	Coun	ter 0	Сс	ontrol F	Registe
Bit			7	6	5		4	3		2	1		0	
		F	0C0	WGM00	COM01	CC	00M00	WGM01	0	S02	CS01	1	CS00	TCCR0
Read/Wr	ite		W	R/W	R/W	F	R/W	R/W	I	R/W	R/W		R/W	1
nitial Va	lue		0	0	0		0	0		0	0		0	
Mode	WGM (CTC	101 :0)	WGM (PWN	00 Time 10) of O	er/Counter Me	ode	тор	Update OCR0	of	TOV0 Set-o	Flag n			
0	0		0	Norr	nal		0xFF	Immedi	ate	MAX				
1	0		1	PWM	1, Phase Corr	ect	0xFF	TOP		BOTT	ом			
2	1		0	стс			OCR0	Immedi	ate	MAX				
3	1		1	Fast	PWM		0xFF	BOTTO	М	MAX				
COM	01	со	00M00	Descrip	tion									
0			0	Normal	oort operation	, 000) disconn	ected.						
0			1	Reserve	d									
1			0	Clear O (non-inv	C0 on compar erting mode)	e mat	tch, set C	C0 at BOT	TON	И,				
1			1	Set OCO (inverting	on compare g mode)	match	n, clear O	C0 at BOT	TON	1,				

- table COM 01:00 is for the Fast PWM mode
- we choose WGM 01:00 = 11, COM 01:00 = 10 CS 02:00 = 100
- the final value is: TCCR0 = 01101100 = 6Ch

Code Wizard VR - untitled.cwp File Help USART Analog Comparator ADC SPI 12C 1 Wire 2 Wire (12C) LCD Bit-Banged Project Information Chip Ports External IRQ Timers Timer 0 Timer 1 Timer 2 Watchdog Clock Source: System Clock Clock Value: 13.184 kHz		
Mode: Fast PWM top=FFh Output: Non-Inverted PWM □ verflow Interrupt □ compare Match Interrupt Timer Value: 0 h Compare: 0	Code Wizard	CodeWizar dAVR - untitled.cwp File Help USART Analog Comparator ADC SPI 12C 1 Wire 2 Wire (12C) LCD Bit-Banged Project Information Chip Ports External IRQ Timers Timer 0 Timer 1 Timer 2 Watchdog Clock Source: System Clock Clock Value: 13.184 kHz Mode: Fast PWM top=FFh Output: Non-Inverted PWM Qverflow Interrupt Compare Match Interrupt Timer Value: 0 h Compare: 0 h

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```
Sample program in PWM mode
// timer0 init in PWM
// Clock source: System Clock/256, Clock value: 52734 Hz, Mode: Fast PWM top=FFh, OC0:
    Non-Inverted PWM
TCCR0=0x6C;
TCNT0=0x00;
OCR0=0x00;
// 4 different light intensities for LED, set using 4 different values of the OCR0 register
// pause 1 second between each intensity change
void main (void)
{
    while(TRUE)
    {
         OCR0 = 0; delay_ms(1000);
                                                // no light
         OCR0 = 4; delay_ms(1000);
                                                // little light
         OCR0 = 16; delay_ms(1000);
                                                // medium light
         OCR0 = 253; delay_ms(1000); // full light
    }
}
                                                                                    25
```