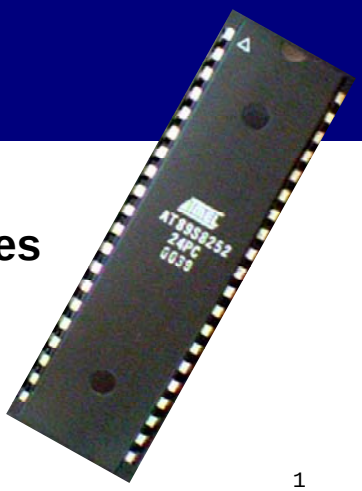
ATmega16A Microcontroller

Chapter 6. AVR Overview, CPU, Memories



What does AVR RISC mean?

- The acronym **AVR** has been reported to stand for: **A**dvanced **V**irtual **R**ISC
- **RISC** stands for reduced instruction set computer.
  - CPU design with a reduced instruction set as well as a simpler set of instructions (like for example PIC and AVR)
- Harvard architecture
  - separate bus for program and data memory

AVR 8-Bit RISC High Performance

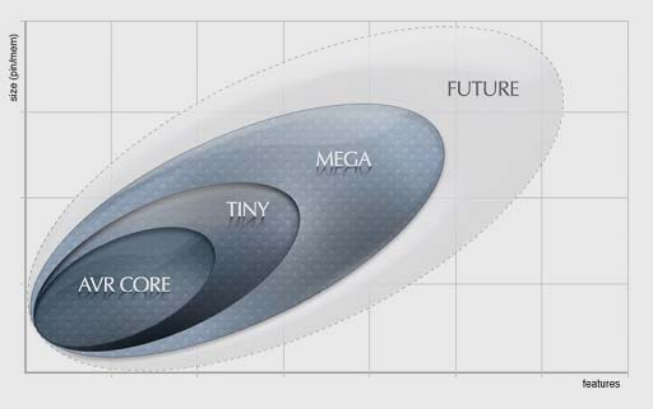
- True single cycle execution
  - single-clock-cycle-per-instruction execution
  - PIC microcontrollers take 4 clock cycles/instruction
- One MIPS (mega instructions per second) per MHz (up to 20 MHz clock).
- 32 general purpose registers
  - provide flexibility and performance when using high level languages
  - prevents access to RAM

AVR 8-Bit RISC Low Power Consumption

- 1.8 to 5.5V operation
  - will use all the energy stored in your batteries
- A variety of sleep modes
  - AVR Flash microcontrollers have up to six different sleep modes
  - fast wake-up from sleep modes
- Software controlled frequency

AVR 8-Bit RISC Compatibility

- AVR® Flash microcontrollers share a single core architecture
  - use the same code for all families
  - 1 Kbytes to 256 Kbytes of code
  - 8 to 100 pins
  - all devices have Internal oscillators



AVR 8-Bit RISC family

- **tinyAVR**
  - 1-16 KBytes Flash, 8-32 pin
- **megaAVR**
  - 4-256 KBytes Flash, 28-100 pin
  - Extended instructions (multiplication)
- **XMEGA**
  - 16-384 KBytes Flash, 44-100 pin
  - Extra: DMA, coding support
- **AVR ASIC**
  - megaAVR with LCD, USB, CAN interfaces.

Most Importantly!!!

- Best C compiler to start programming in C
  - and it is FREE
- Code Vision AVR
  - http://www.hpinfotech.ro/
- AVR Studio 4 also free from:
  - http://www.atmel.com/dyn/products/tools_card.asp?tool_id=2725

ATmega16A features

- Advanced RISC Architecture
  - 131 Powerful Instructions – Most Single-clock Cycle Execution
  - 32 x 8 General Purpose Working Registers
  - Up to 16 MIPS at 16 MHz
  - On-chip 2-cycle Multiplier

ATmega16A features

- Memory segments
  - 16K Bytes of In-System Self-programmable Flash program memory
  - 512 Bytes EEPROM (**E**lectrically **E**rasable **P**rogrammable **R**ead-**O**nly **M**emory)
  - 1K Byte Internal SRAM (**S**tatic **R**andom **A**ccess **M**emory)
  - Write/Erase Cycles: 10,000 Flash/100,000 EEPROM

ATmega16A features

- Peripheral features
  - Two 8-bit Timer/Counters and one 16-bit Timer/Counter with Separate Prescalers, Compare Mode and Capture Mode
  - Real Time Counter with Separate Oscillator
  - Four PWM Channels
  - 8-channel, 10-bit ADC

ATmega16A features

- Peripheral features
  - Byte-oriented Two-wire Serial Interface
  - Programmable Serial USART
  - Master/Slave SPI Serial Interface
  - Programmable Watchdog Timer
  - On-chip Analog Comparator

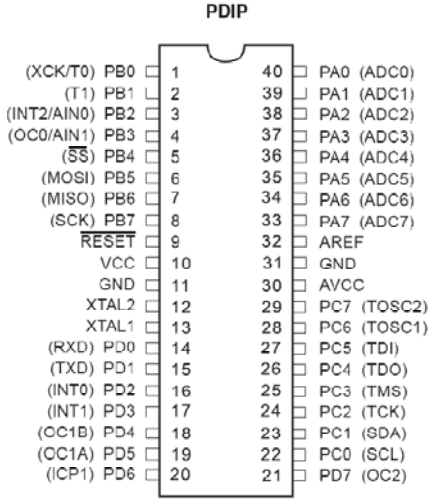
ATmega16A features

- Special Microcontroller Features
  - Power-on Reset and Programmable Brown-out Detection
  - Internal Calibrated RC Oscillator
  - External and Internal Interrupt Sources
  - Six Sleep Modes

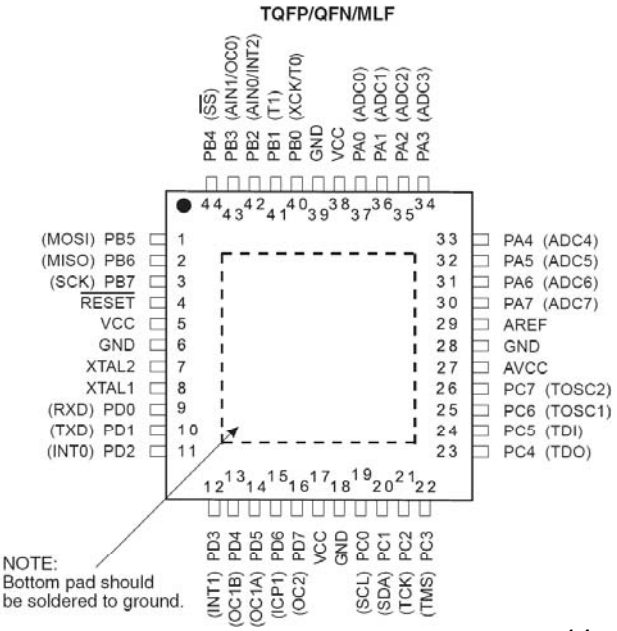
ATmega16A features

- I/O and Packages
  - 32 Programmable I/O Lines
  - 40-pin PDIP, 44-lead TQFP, and 44-pad QFN/MLF
- Operating Voltages
  - 2.7 - 5.5V for ATmega16A
- Power Consumption (1 MHz, 3V, and 25°C)
  - Active: 0.6 mA
  - Idle Mode: 0.2 mA

- Plastic Dual Inline Package (PDIP)

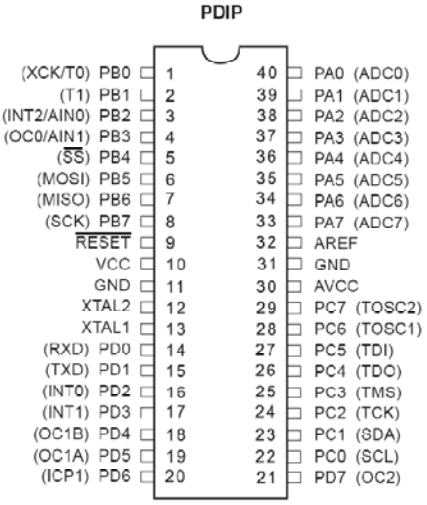


- Thin Profile Plastic Quad Flat Package (TQFP)
- Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)



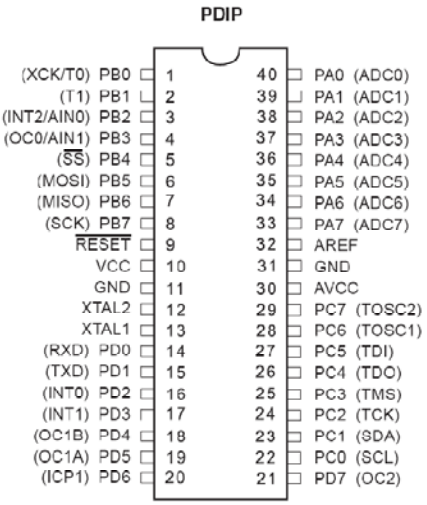
Pin Configurations

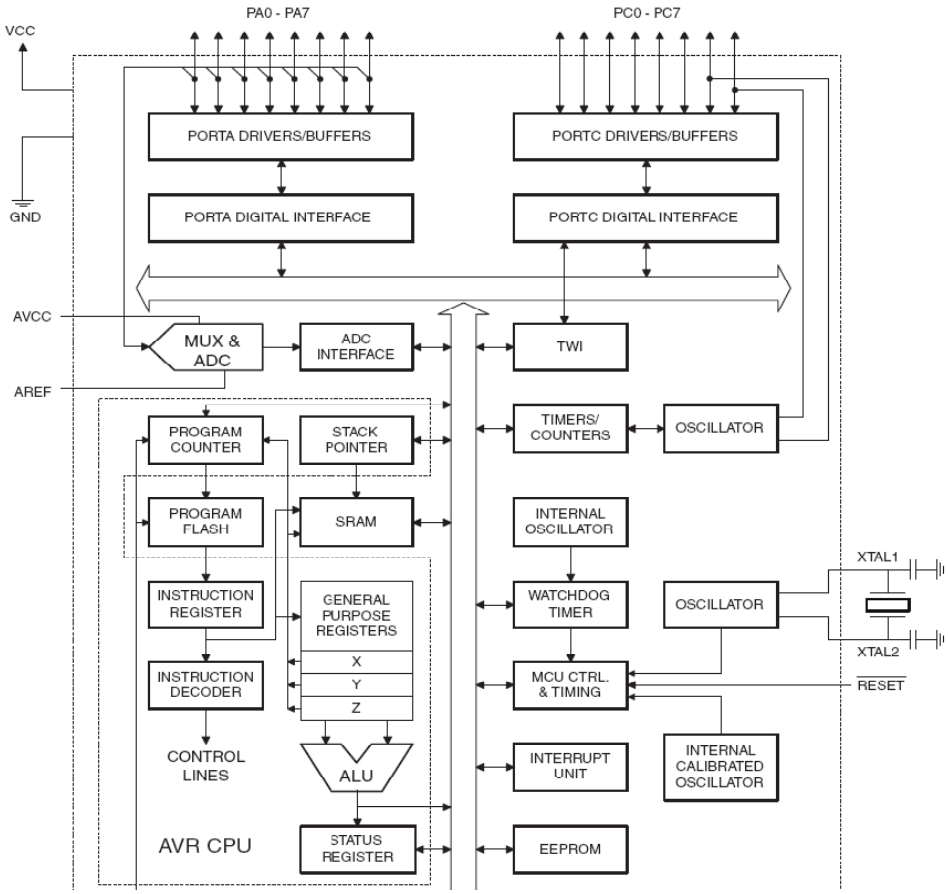
- **VCC -** Digital supply voltage
- **GND -** Ground
- **Port A (PA7:PA0)**
  - analog inputs to the A/D Converter
  - 8-bit bi-directional I/O port (if the A/D Converter is not used)
- **Port B (PB7:PB0)**
  - 8-bit bi-directional I/O port
  - functions of various special features
- **Port C (PC7:PC0)**
  - 8-bit bi-directional I/O port
  - JTAG interface (Standard Test Access Port and Boundary-Scan)

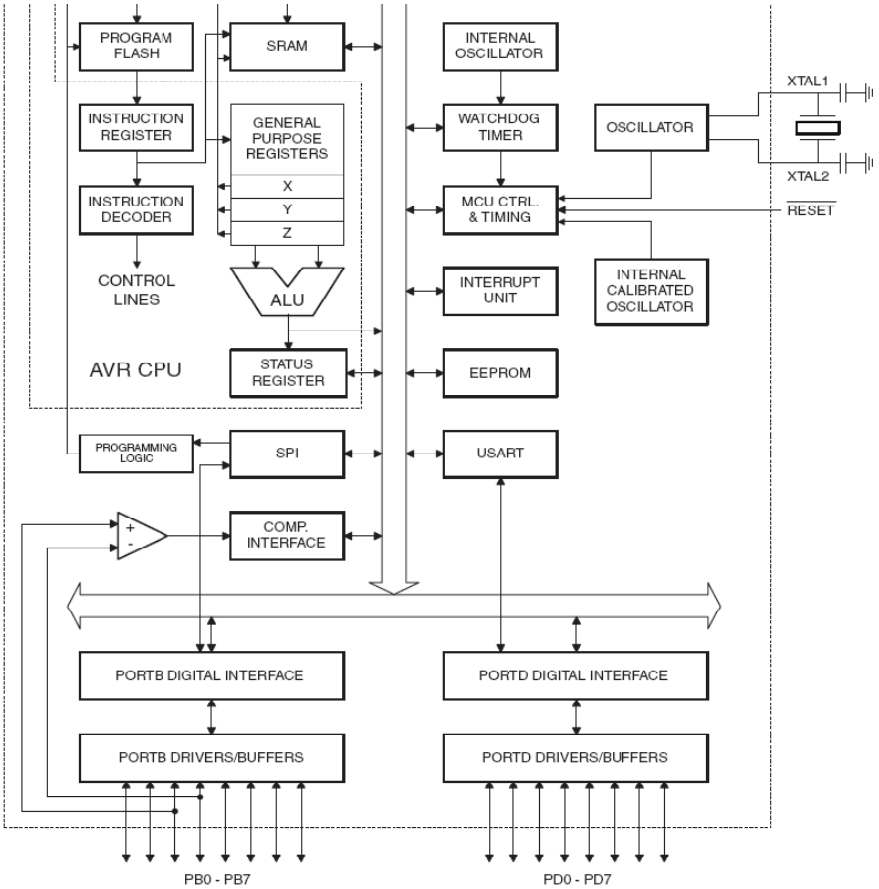


Pin Configurations

- **Port D (PD7:PD0)**
  - 8-bit bi-directional I/O port
  - functions of various special features
- **RESET**
  - Reset Input. A low level active
- **XTAL1, XTAL2**
  - oscilator pins
- **AVCC**
  - the supply voltage pin for Port A and the A/D Converter
- **AREF**
  - analog reference voltage for ADC




PA0 - PA7
PC0 - PC7
VCC
GND
PORTA DRIVERS/BUFFERS
PORTC DRIVERS/BUFFERS
PORTA DIGITAL INTERFACE
PORTC DIGITAL INTERFACE
AVCC
AREF
MUX & ADC
ADC INTERFACE
TWI
PROGRAM COUNTER
STACK POINTER
TIMERS/ COUNTERS
OSCILLATOR
PROGRAM FLASH
SRAM
INTERNAL OSCILLATOR
INSTRUCTION REGISTER
GENERAL PURPOSE REGISTERS
X
Y
Z
WATCHDOG TIMER
OSCILLATOR
XTAL1
XTAL2
INSTRUCTION DECODER
MCU CTRL. & TIMING
RESET
CONTROL LINES
ALU
INTERRUPT UNIT
INTERNAL CALIBRATED OSCILLATOR
AVR CPU
STATUS REGISTER
EEPROM


PROGRAM FLASH
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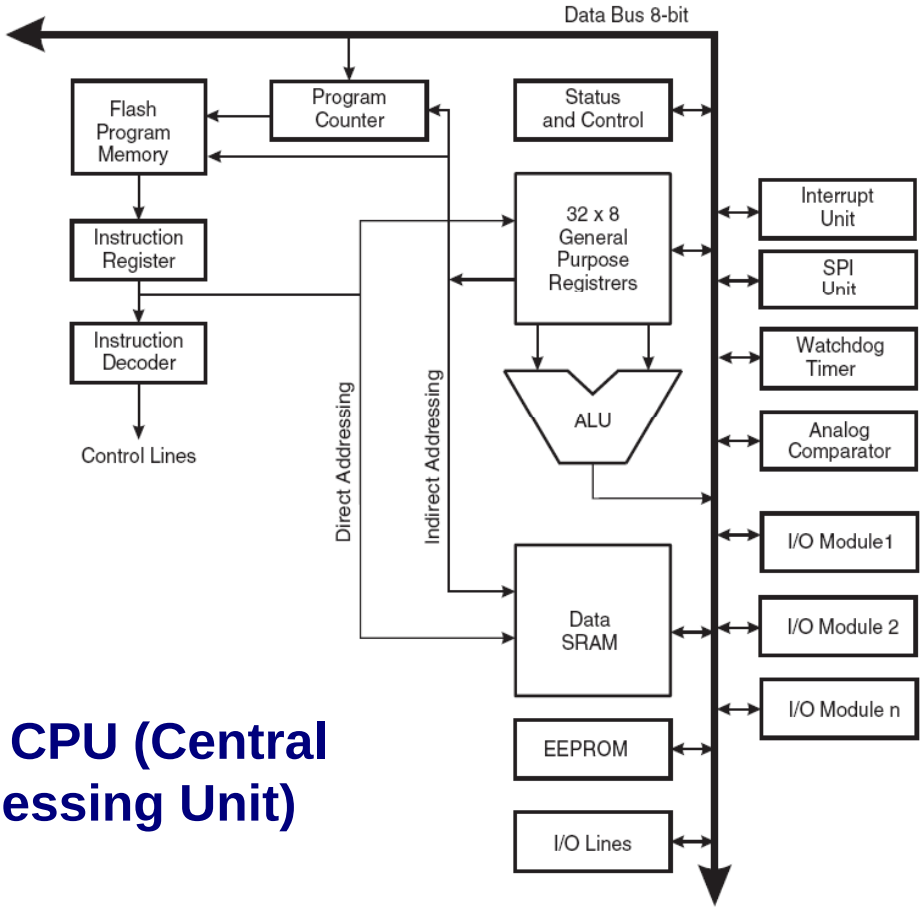
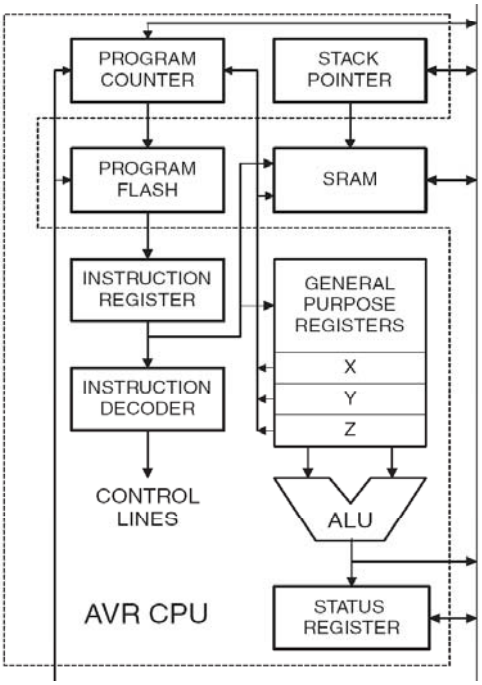
STATUS REGISTER
EEPROM
PROGRAMMING LOGIC
SPI
USART
COMP. INTERFACE
PORTB DIGITAL INTERFACE
PORTD DIGITAL INTERFACE
PORTB DRIVERS/BUFFERS
PORTD DRIVERS/BUFFERS
PB0 - PB7
PD0 - PD7



AVR CPU (Central Processing Unit)

AVR CPU

- AVR uses a Harvard architecture
  - separate memories and buses for program and data
- The program memory is In-System Reprogrammable Flash memory
- 32 x 8-bit general purpose registers
  - single-cycle Arithmetic Logic Unit (ALU) operation
  - 6 registers can be used as three 16-bit indirect address register pointers



Status Register

Bit	7	6	5	4	3	2	1	0	
	I	T	H	S	V	N	Z	C	SREG
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – I: Global Interrupt Enable**
  - 1=enable, 0=disable interrupts
- **Bit 6 – T: Bit Copy Storage**
  - source or destination for the operated bit
- **Bit 5 – H: Half Carry Flag**
- **Bit 4 – S: Sign Bit, S = N⊕V**
- **Bit 3 – V: Two's Complement Overflow Flag**
- **Bit 2 – N: Negative Flag**
  - 1=negative,0=positive result
- **Bit 1 – Z: Zero Flag**
  - 1=zero result
- **Bit 0 – C: Carry Flag**

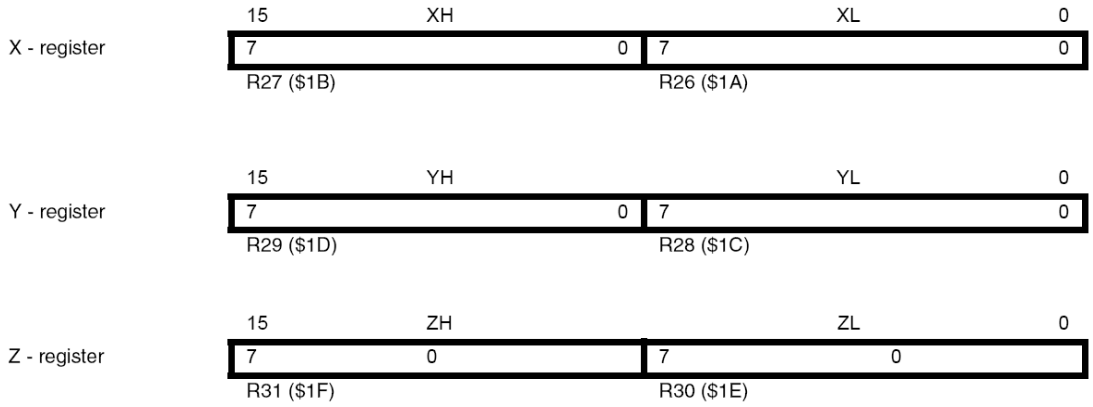
General Purpose Register File

7 0	Addr.	
R0	$00	
R1	$01	
R2	$02	
…		
R13	$0D	
R14	$0E	
R15	$0F	
R16	$10	
R17	$11	
…		
R26	$1A	X-register Low Byte
R27	$1B	X-register High Byte
R28	$1C	Y-register Low Byte
R29	$1D	Y-register High Byte
R30	$1E	Z-register Low Byte
R31	$1F	Z-register High Byte

- One 8-bit output operand and one 8-bit result input
- Two 8-bit output operands and one 8-bit result input
- Two 8-bit output operands and one 16-bit result input
- One 16-bit output operand and one 16-bit result input

The X-register, Y-register and Z-register

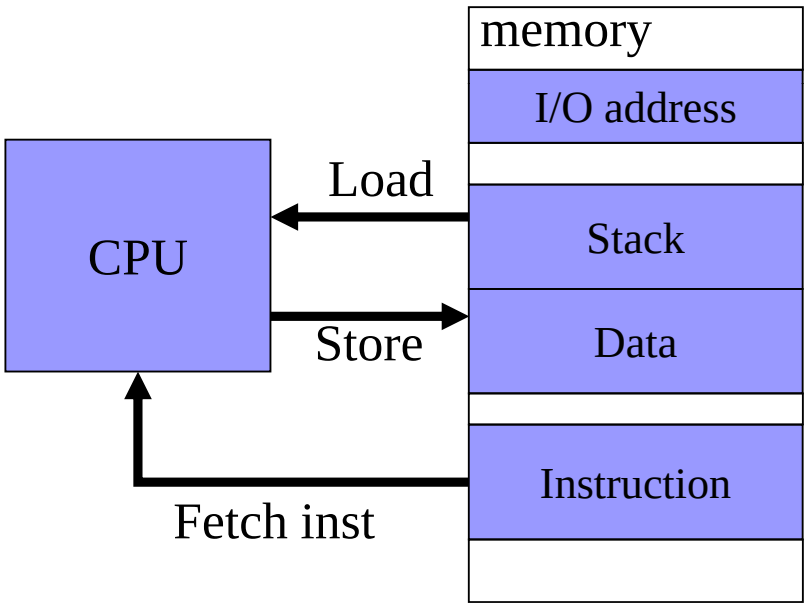
- The registers R26:R31 can be used as 16-bit address pointers for indirect addressing of Data Space



Major Instruction Types

- **Arithmetic and logic:**
  - add, subtract, multiply;
  - and, or, not, xor
- **Data movement:**
  - transfer data between registers and/or memories
- **Control:**
  - Branches and jumps

Instruction Execution



Register Instructions

- Data copying

```
mov  r4, r7
```

- Immediate values

```
ldi  r16, 5
ori  r16, 0xF0
andi r16, 0x80
subi r20, 1
```

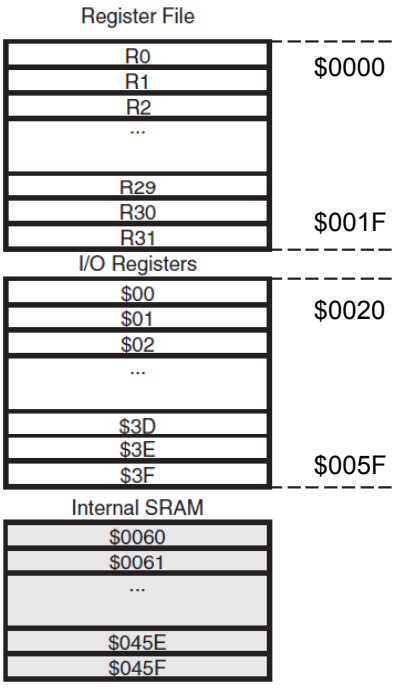
Register Instructions

- Arithmetic and Logic registers operations

```
add r1, r2
or  r3, r4
lsl r5
mul r5, r18  ; r1:r0 = r5*r18
rol r7
ror r9
inc r19
dec r17
```


AVR Data Memory

- 32 general purpose working registers,
- 64 I/O Registers,
- 1024 bytes of internal data SRAM



Data memory instructions

- Direct addressing

```
lds r3, 0x10FE
lsl r3
sts 0x10FE, r3
```

- Indirect addressing
  - the base address given by the Y- or Z-register

```
ldi r27, 0x10      ; X upper byte is r27
ldi r26, 0xFE      ; X lower byte is r26
ld r0, X
lsl r0
st X, r0
```

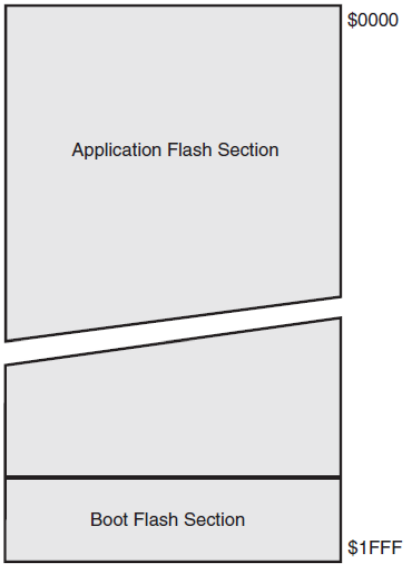

Data memory instructions

- Indirect addressing modes with automatic pre-decrement and post-increment

```
ld r0, X+       ; memory access at address X,
                ; then X is incremented
ld r0, +X       ; X is incremented
                ; then memory access at address X
ld r0, X-
ld r0, -X
```

AVR Program Memory

- 16K bytes On-chip Flash memory for program storage
- Organized as 8K x 16
- Divided into two sections,
  - Boot Program sectio
  - Application Program section
- At least 10,000 write/erase cycles



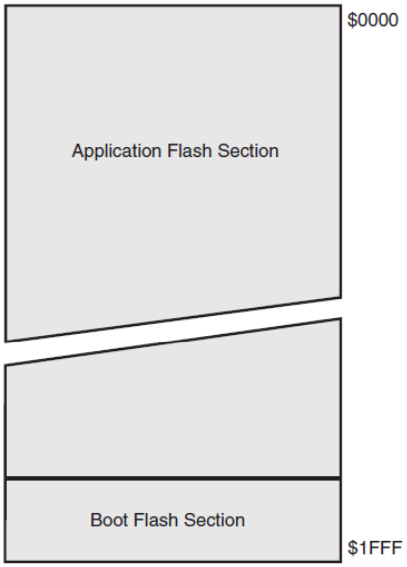
AVR Program Memory

- Read
  - **BYTE access**
  - Addressing by Z pointer

```
LPM r5, Z
LPM r5, Z+
LPM     ; r0 este destinatie,
        ; Z adresa
```

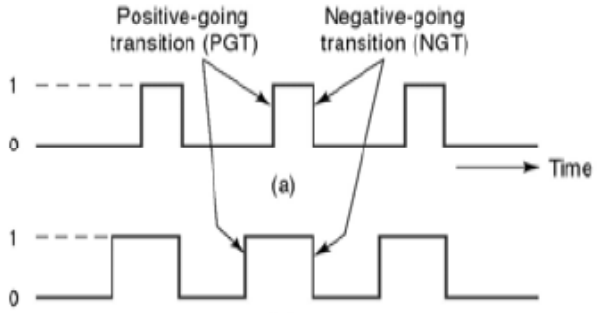
- Write **– word only**

```
SPM     ; PM(Z) <= R1:R0
```



Clock signal

- A clock signal is a square wave of fixed frequency f_{CK}
- Often, transitions will occur on one of the edges of clock pulses
  - the rising edge
  - the falling edge

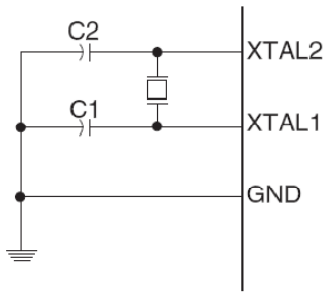


Clock Sources – AVR uC

- External Crystal/Ceramic Resonator
- External Low-frequency Crystal
- External RC Oscillator
- Calibrated Internal RC Oscillator
- External Clock

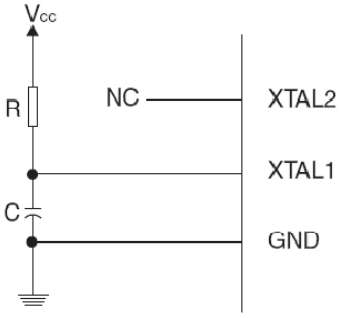
Clock Sources – AVR uC

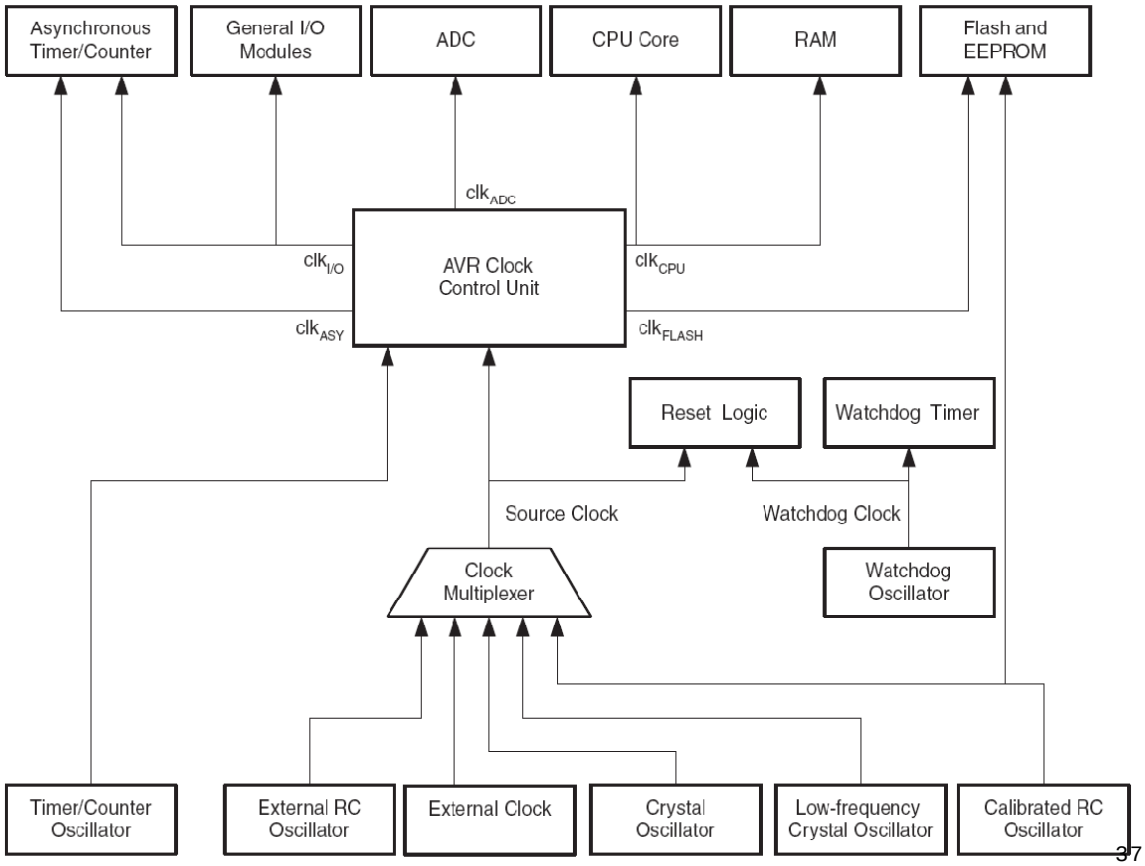
- External Crystal/Ceramic Resonator
  - 0.4 - 0.9 MHz (Ceramic Resonator)
  - 0.9 - 3.0 MHz
  - 3.0 - 8.0 MHz
  - ≤ 1.0 MHz
- External Low-frequency Crystal
  - watch crystal 32.768 kHz



Clock Sources – AVR uC

- External RC Oscillator
  - 0.1 - 0.9 MHz
  - 0.9 - 3.0 MHz
  - 3.0 - 8.0 MHz
  - 8.0 - 12.0 MHz
- Calibrated Internal RC Oscillator
  - 1 MHz (default), 2 MHz, 4 MHz or 8 MHz
- External Clock Drive
  - aplicat direct pe pinul XTAL1




Asynchronous Timer/Counter
General I/O Modules
ADC
CPU Core
RAM
Flash and EEPROM
clk_ADC
clk_I/O
AVR Clock Control Unit
clk_CPU
clk_ASY
clk_FLASH
Reset Logic
Watchdog Timer
Source Clock
Watchdog Clock
Clock Multiplexer
Watchdog Oscillator
Timer/Counter Oscillator
External RC Oscillator
External Clock
Crystal Oscillator
Low-frequency Crystal Oscillator
Calibrated RC Oscillator