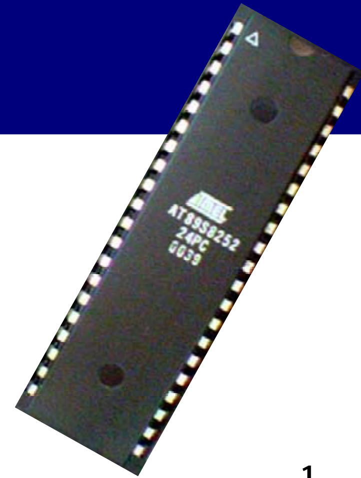
Digital Integrated Circuits & Microcontrollers

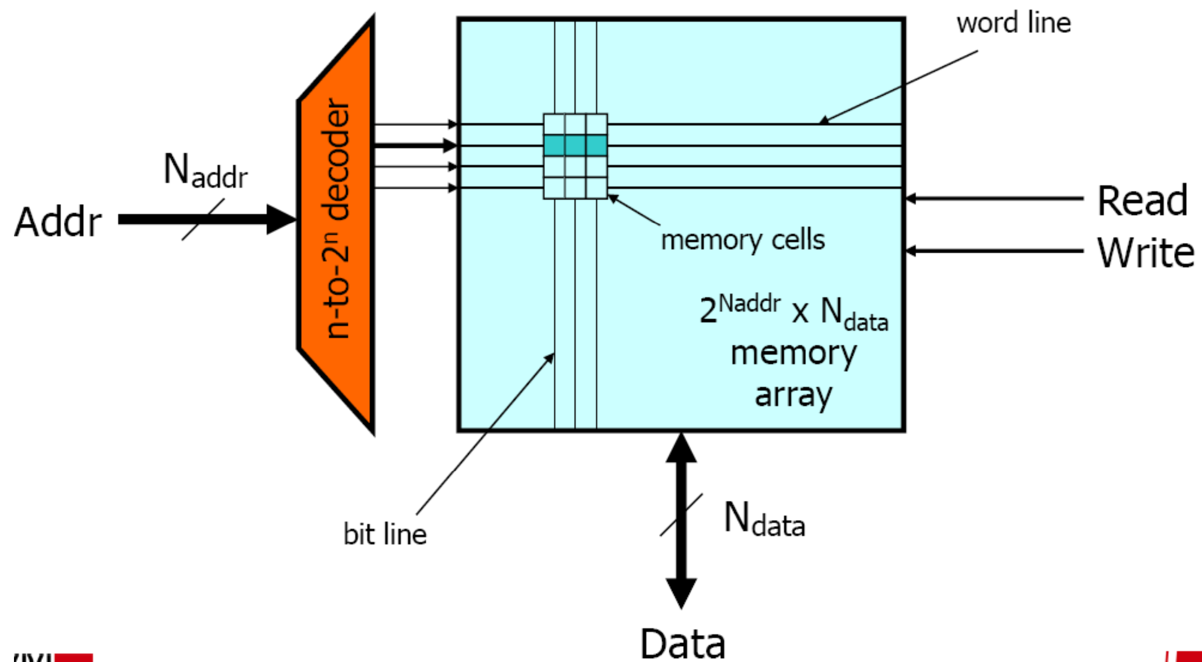


Chapter 5. Semiconductor Memories

Memories

- Bits of information arranged into arrays
  - Each row is an item of information and is identified by an **Address**
  - The set of bits identified by the same address belong to a **Word**
- The number of addresses is often a power of two;
- The number of bits in a word is sometimes a multiple of four or eight, or arbitrary

Memory organization



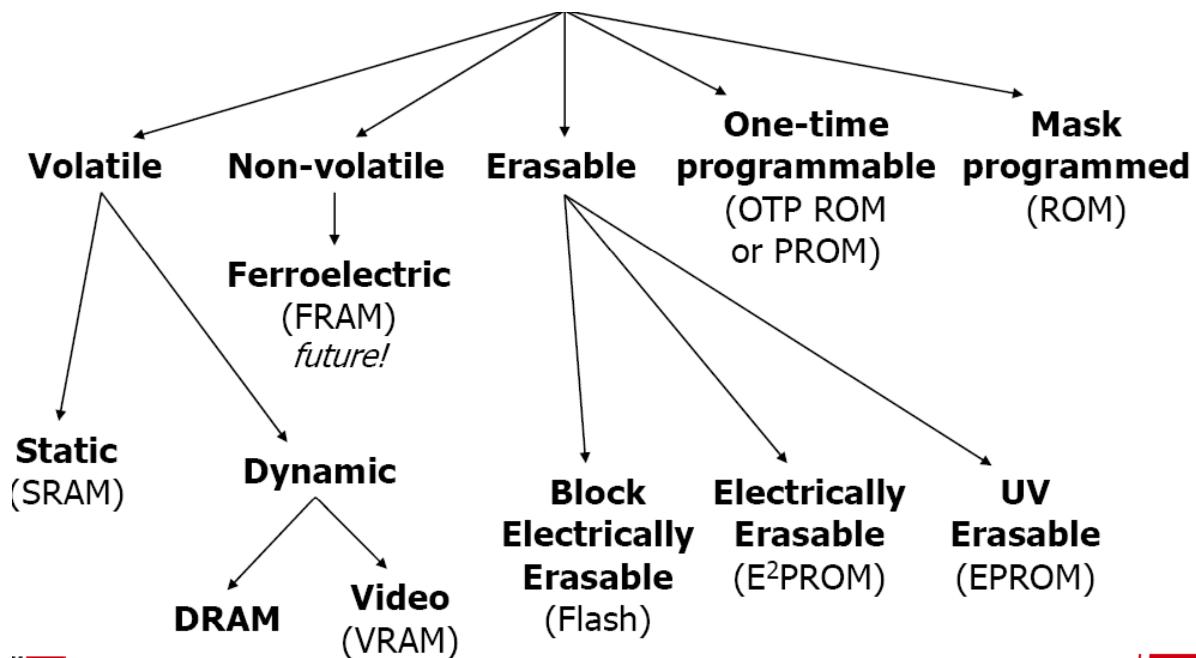
Memory Basics

- RAM: Random Access Memory
  - historically defined as memory array with individual bit access
  - refers to memory with both Read and Write capabilities
- ROM: Read Only Memory
  - no capabilities for “online” memory Write operations
  - Write typically requires high voltages or erasing by UV light

Memory Basics

- Volatility of Memory
  - volatile memory loses data over time or when power is removed
    - RAM is volatile
  - non volatile memory stores date even when power is removed
    - ROM is non-volatile
- Static vs. Dynamic Memory
  - Static: holds data as long as power is applied (SRAM)
  - Dynamic: will lose data unless refreshed periodically (DRAM)

Memory Types



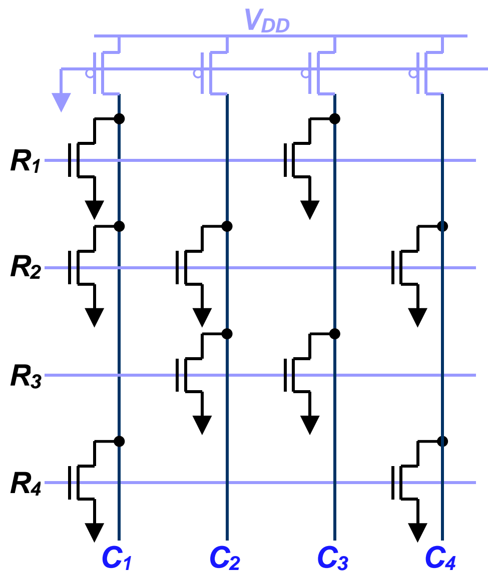
ROM: Read Only Memory

- Nonvolatile memories
- Only can access data, cannot to modify data
- Lower cost: used for permanent memory in printers, fax, and game machines, and ID cards
- Typical applications:
  - store the microcoded instructions set of a microprocessor
  - store a portion of the operation system for PCs
  - store the fixed programs for microcontrollers (firmware)

ROM: Read Only Memory

- PROM: Programmable Read Only Memory
    - programmable by user -using special program tools/modes
    - read only memory -during normal use
    - non-volatile
  - Read Operation
    - like any ROM: address bits select output bit combinations
  - Write Operation
    - typically requires high voltage (~15V) control inputs to set data
  - Erase Operation
    - EPROM: erasable PROM: uses UV light to reset all bits
    - EEPROM: electrically-erasable PROM, erase with control voltage

4bit × 4Bit NOR-based ROM Array

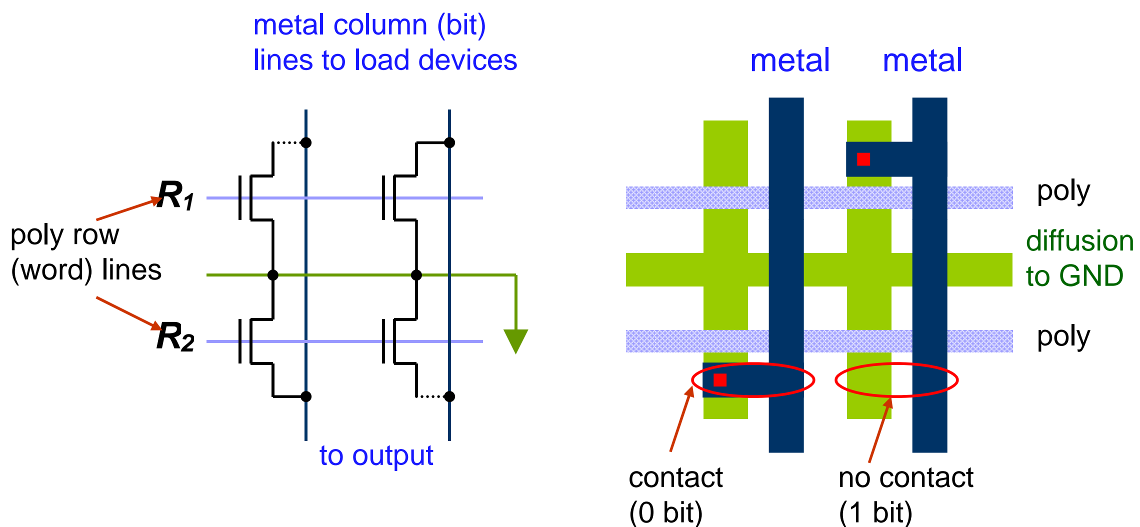


- "1" bit stored - absence of an active transistor
- "0" bit stored - presence of an active transistor

R_1	R_2	R_3	R_4	C_1	C_2	C_3	C_4
1	0	0	0	0	1	0	1
0	1	0	0	0	0	1	1
0	0	1	0	1	0	0	1
0	0	0	1	0	1	1	0

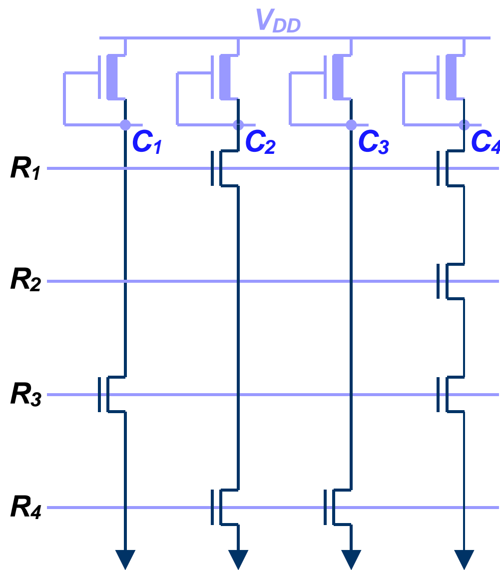
A word is selected by rising to "1" the corresponding wordline

Contact-Mask Programmable NOR ROM



- **"0" bit:** drain is connected to metal line via a metal-to-diffusion contact
- **"1" bit:** omission the connect between drain and metal line.

4Bit × 4Bit NAND-based ROM Array



- "1" bit stored - presence of a transistor that can be switched off
- "0" bit stored - shorted / normally-on transistor

R_1	R_2	R_3	R_4	C_1	C_2	C_3	C_4
0	1	1	1	0	1	0	1
1	0	1	1	0	0	1	1
1	1	0	1	1	0	0	1
1	1	1	0	0	1	1	0

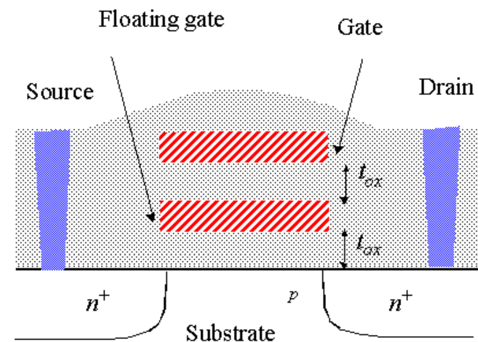
A word is selected by putting to "0" the corresponding wordline R_i

Nonvolatile Read-Write Memories

- The architecture is similar to the ROM structure
  - Array of transistors placed on a word-line/bit-line grid
  - Special transistor that permits its threshold to be altered electrically
  - Programming: selectively disabling or enabling some of these transistors
  - Reprogramming: erasing the old threshold values and start a new programming cycle

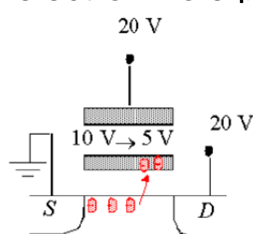
EPROM

- The floating gate avalanche-injection MOS (**FAMOS) transistor:**
- extra polysilicon strip is inserted between the gate and the channel - **floating gate**
- impact: double the gate oxide thickness, reduce the transconductance, increase the threshold voltage
- threshold voltage is programmable by the trapping electrons on the floating gate through avalanche injection

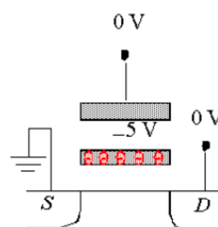


EPROM

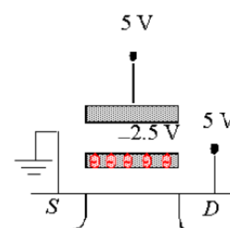
- Electrons acquire sufficient energy to became “hot” and traverse the first oxide insulator so that they get trapped on the floating gate
- Electron accumulation on the floating gate is a self-limiting process that increases the threshold voltage (~7V)
- The trapped charge can be stored for many years
- The erasure is performed by shining strong ultraviolet light on the cells through a transparent window in the package
- The UV radiation renders the oxide conductive by direct generation of electron-hole pairs



Avalanche injection



Removing programming voltage leaves charge trapped



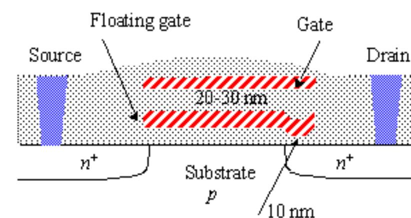
Programming results in higher V_T

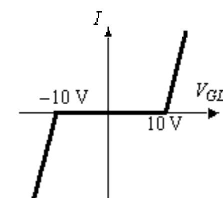
EPROM

- The erasure process is slow (~min.)
- The erasure procedure is **off-system!**
- Programming takes several usecs/word
- Limited endurance - max 1000 erase/program cycles
- The cell is very simple and dense: large memories at low cost!
- Applications that do not require regular reprogramming

EEPROM

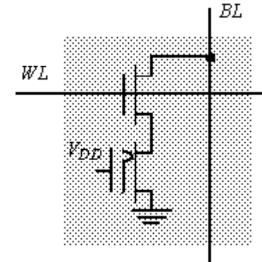
- Provide an electrical-erasure procedure
- Modified floating-gate device, floating-gate tunneling oxide (**FLOTOX):**
- reduce the distance between floating gate and channel near the drain
- Fowler-Nordheim tunneling mechanism (when apply 10V over the thin insulator)





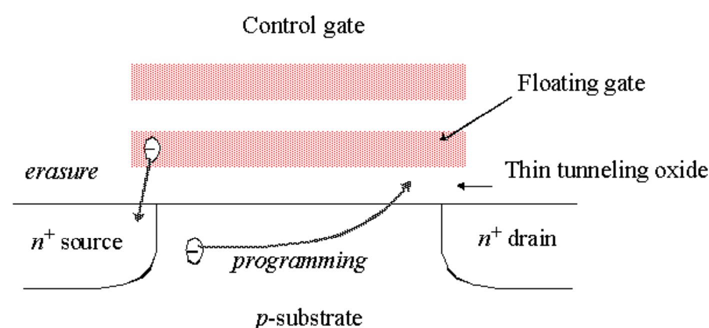
EEPROM

- Reversible programming by reversing the applied voltage (rise and lower the threshold voltage)
  - difficult to control the threshold voltage
  - extra transistor required as access device
- Larger area than EPROM
- More expensive technology than EPROM
- Offers a higher versatility than EPROM
- Can support 105 erase/write cycles



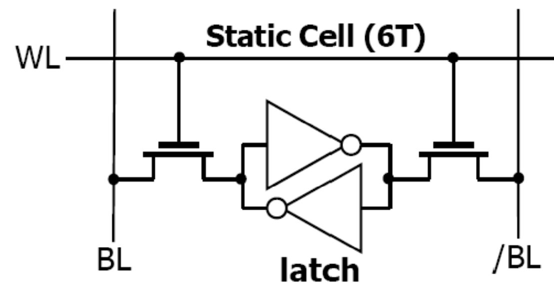
Flash Memories

- Combines the density of the EPROM with the versatility of EEPROM structures
  - Programming: avalanche hot-electron-injection
  - Erasure: Fowler-Nordheim tunneling (like EEPROM)
  - Difference: erasure is performed in bulk for the complete (or subsection of) memory chip



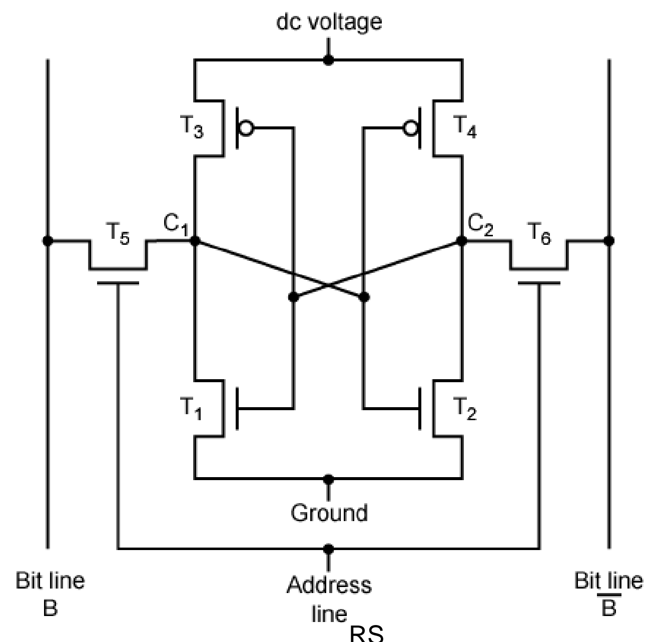
Static RAM (SRAM)

- Permit the modification (writing) of stored data bits
- The stored data can be retained infinitely, without need of any refresh operation
- 3 Operation States: hold, write, read
- Basic 6T (6 transistor) SRAM Cell
  - bistable (cross-coupled) INVs for storage
  - 2 access transistors
  - word line, WL, controls access
    - WL = 0 (hold)
    - WL = 1 (read/write)



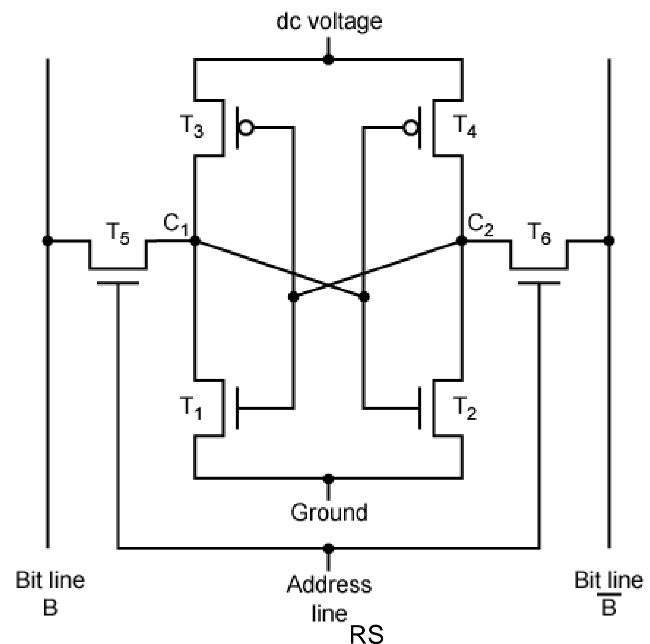
The basic operations on SRAM cells

- RS = 0 (T_5, T_6 off)
  - data is being held
- RS = 1 (T_5, T_6 on)
  - Write "1"
    - $V_{B|}$ - forced to 0 by data write,
    - V_{C2} decreases to 0,
    - T_1 off; V_{C1} increases;
    - Final state: V_{C1}= 1, V_{C2}= 0
  - Read "1"
    - T_1 off; T_2 on;
    - $V_{B|}$ pulled down,
    - $V_B > V_{B|}$ read as a logic "1"



The basic operations on SRAM cells

- RS = 1 (T_5, T_6 on)
  - Write "0"
    - V_B - forced to 0 by data write,
    - V_{C1} decreases to 0,
    - T_2 off; V_{C2} increases to 1;
    - Final state: V_{C1}= 0, V_{C2}= 1
  - Read "0"
    - T_1 on; T_2 off;
    - V_B pulled down,
    - $V_B < V_{B|}$ read as a logic "0"



Dynamic Random Access Memory (DRAM)

- Dynamic: must be refreshed periodically
- Volatile: loses data when power is removed
- 1T DRAM Cell
  - single access transistor;
  - storage capacitor
- control input:
  - word line (WL);
  - data I/O: bit line (BL)