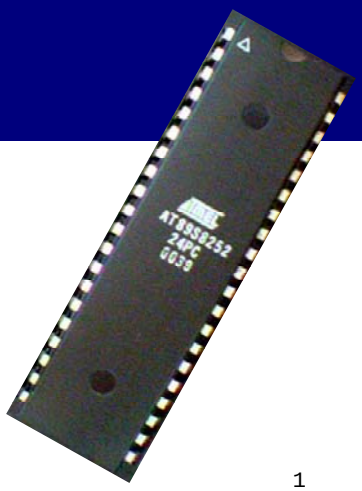
Digital Integrated Circuits & Microcontrollers

Chapter 4. Sequential Digital Circuits



Sequential Circuits

- Combinational Logic
  - the output(s) depends only on the current values of the input variables
- Sequential Logic circuits
  - the output(s) can depend on present and also past values of the input and the output variables
- Sequential circuits exist in one of a defined number of states at any one time
  - they move "sequentially" through a defined sequence of transitions from one state to the next

Synchronous and Asynchronous Sequential Logic

- Synchronous
  - the timing of all state transitions is controlled by a common clock
  - changes in all variables occur simultaneously
- Asynchronous
  - state transitions occur independently of any clock and normally dependent on the timing of transitions in the input variables
  - changes in more than one output do not necessarily occur simultaneously

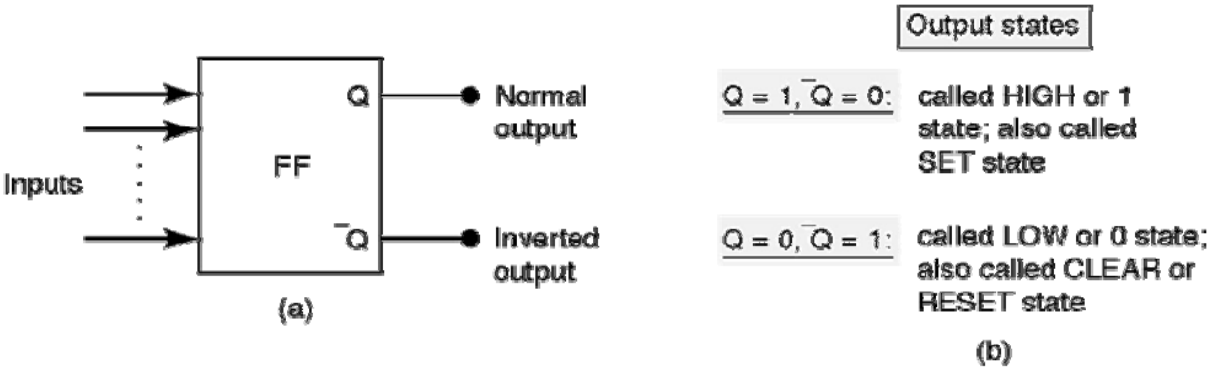
Clock

- A clock signal is a square wave of fixed frequency
- Often, transitions will occur on one of the edges of clock pulses (i.e. the rising edge or the falling edge)

Flip-Flops

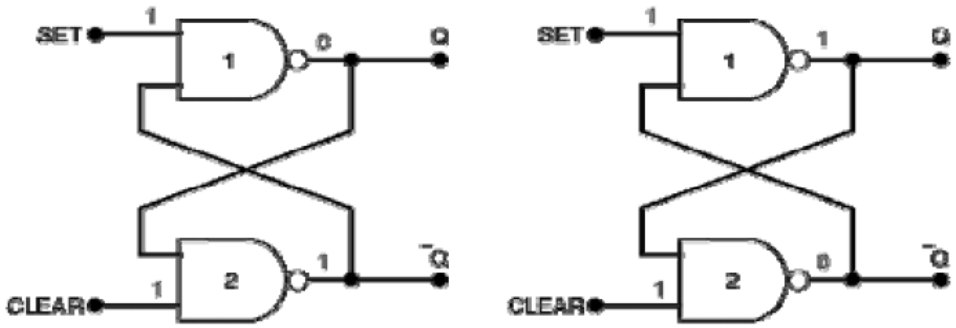
- Flip-flops (bistable) are the fundamental element of sequential circuits
- Flip-flops are essentially 1-bit storage devices
  - outputs can be set to store either 0 or 1 depending on the inputs
  - even when the inputs are de-asserted, the outputs retain their prescribed value
- Three main types of flip-flop:
  - SR, J-K, D

Flip-Flops



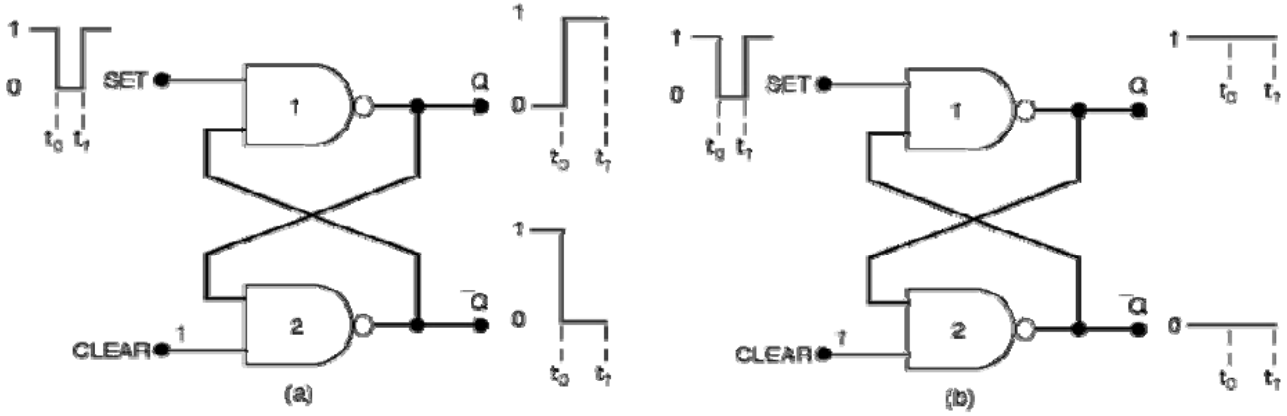
- **Flip-flop (FF) = latch = bistable circuit**

NAND SR Latch



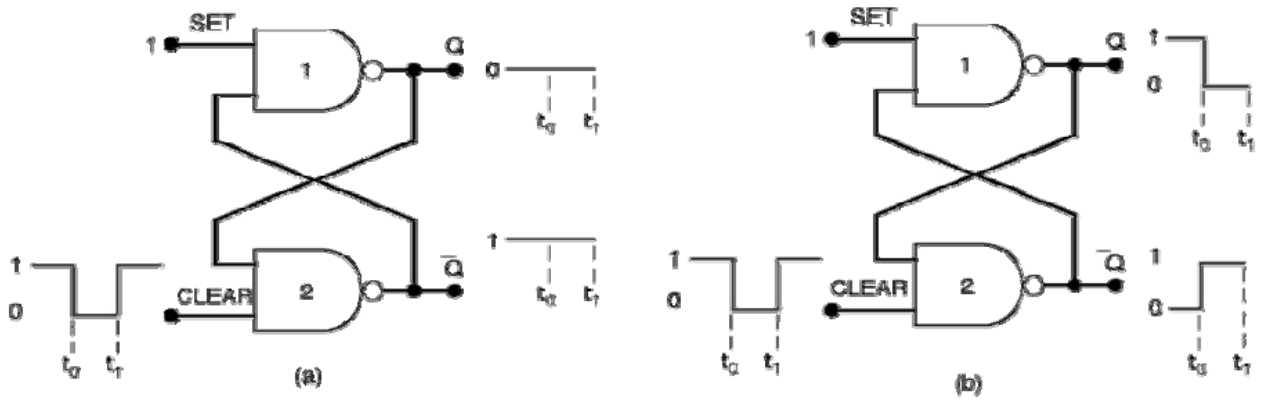
- A NAND latch has two possible resting states when SET = CLEAR = 1

NAND SR Latch



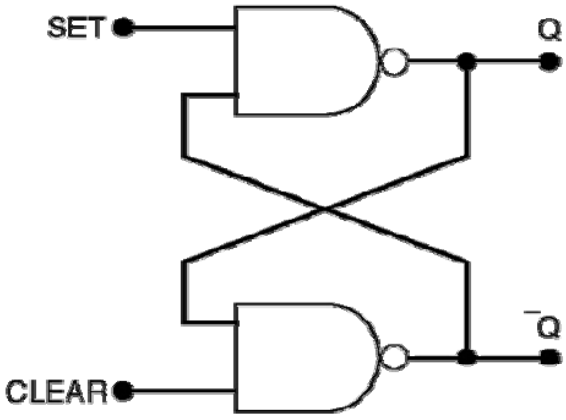
- Negative Pulse on SET input put the latch in a HIGH (SET) state

NAND SR Latch



- Negative Pulse on CLEAR input put the latch in a LOW (Clear or RESET) state.

NAND SR Latch



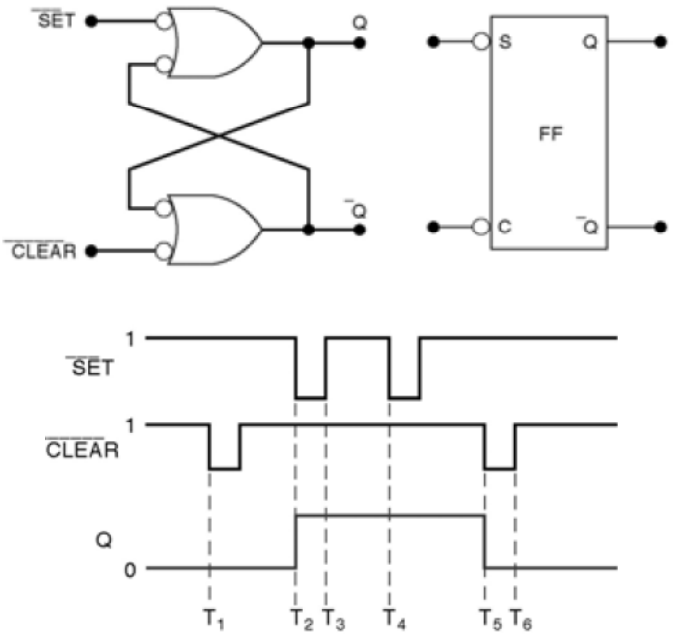
Set	Clear	Output
1	1	No change
0	1	Q = 1
1	0	Q = 0
0	0	Invalid*

*produces Q = $\overline{Q}$ = 1

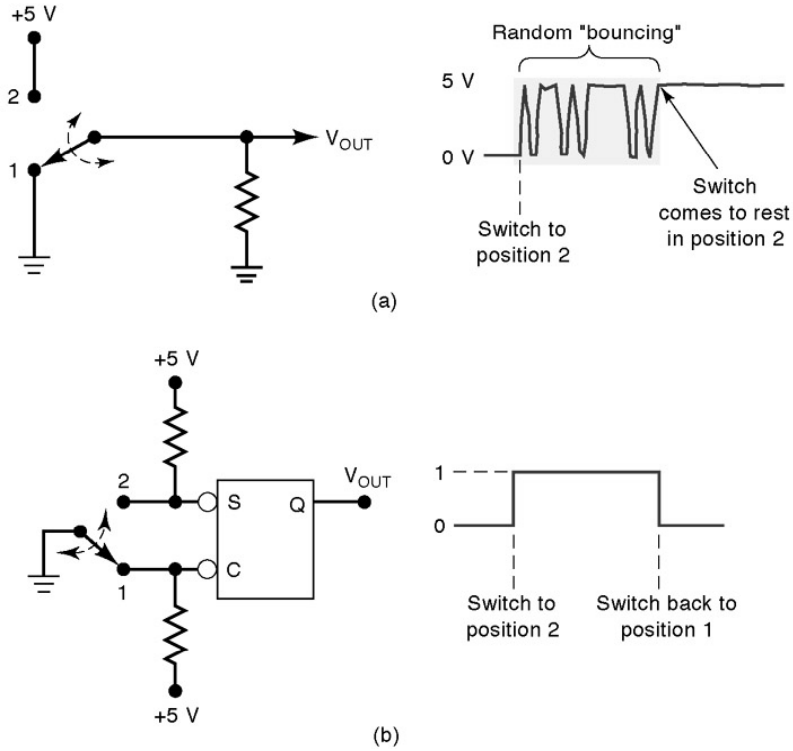
(b)

- Truth table for the NAND Set-Clear (Set-Reset or SR) Latch

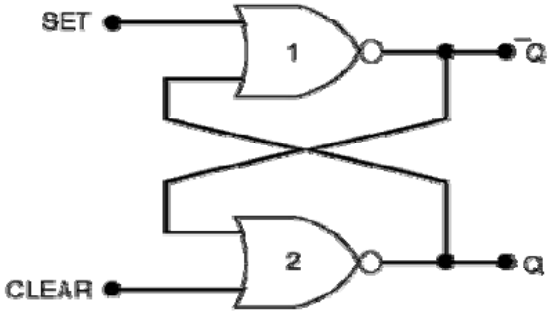
NAND SR Latch



NAND SR Latch to deglitch a switch



NOR SR Latch

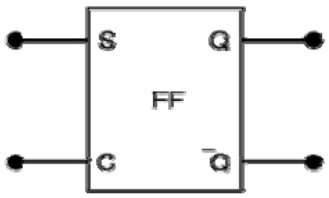


(a)

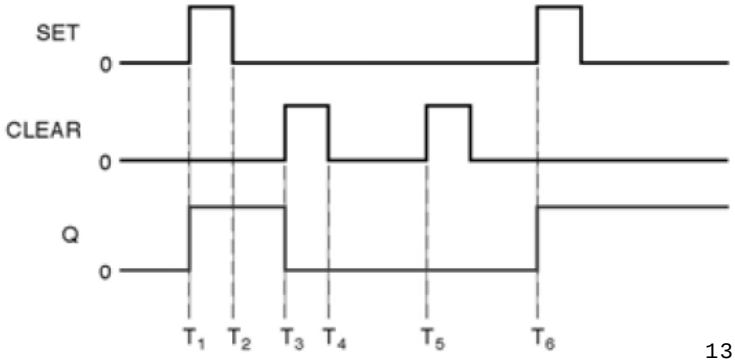
Set	Clear	Output
0	0	No change
1	0	Q = 1
0	1	Q = 0
1	1	Invalid*

*produces $Q = \bar{Q} = 0$

(b)



(c)

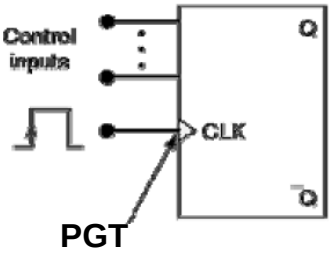


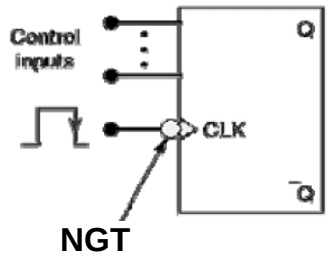
Clocked Flip-Flop Circuits

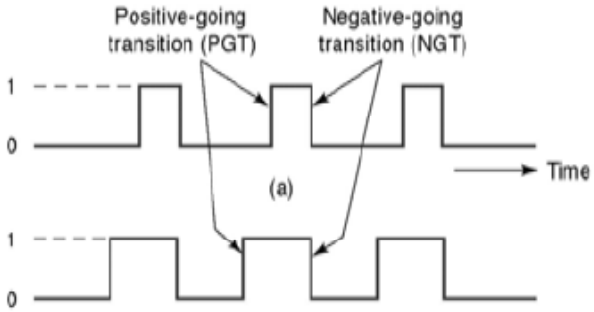
- Digital systems can operate
  - ***Asynchronously*:** output can change state whenever inputs change
  - ***Synchronously*:** output only change state at clock transitions (edges)

Clocked Flip-Flop Circuits

- **Clock signal**
  - Outputs change state at the edge (transition) of the input clock
  - Positive-going transitions (**PGT**)
  - Negative-going transitions (**NGT**)

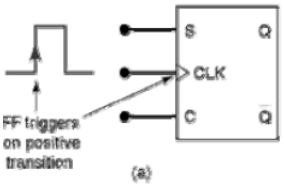






Clocked S-R FF

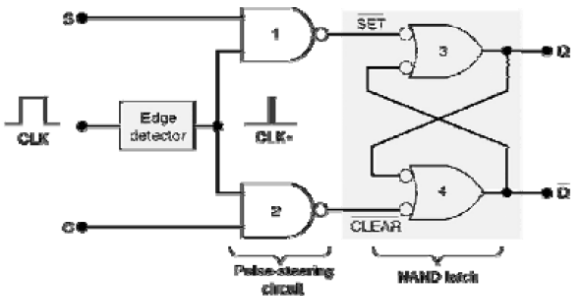
- On positive-going edge of a clock pulse

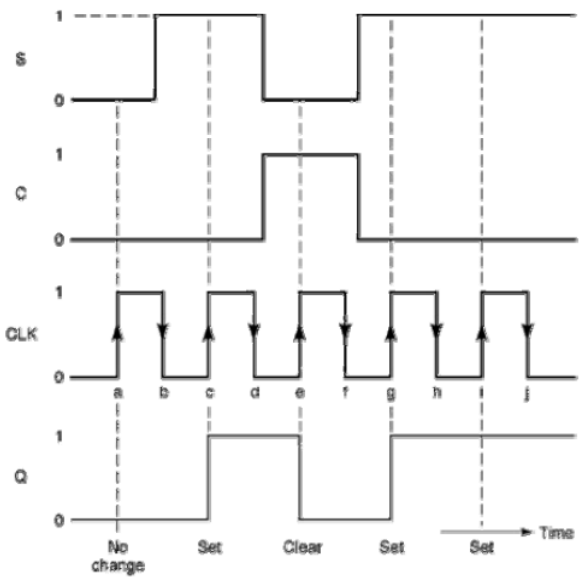


Inputs			Output
S	C	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	Ambiguous

Q_0 is output level prior to ↑ of CLK.
↓ of CLK produces no change in Q.

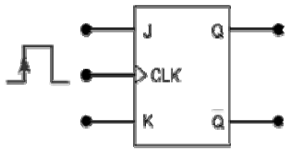
(b)





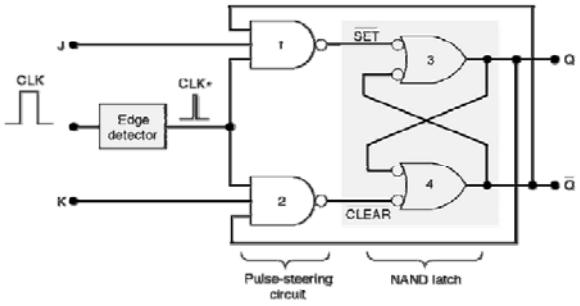
Clocked J-K FF

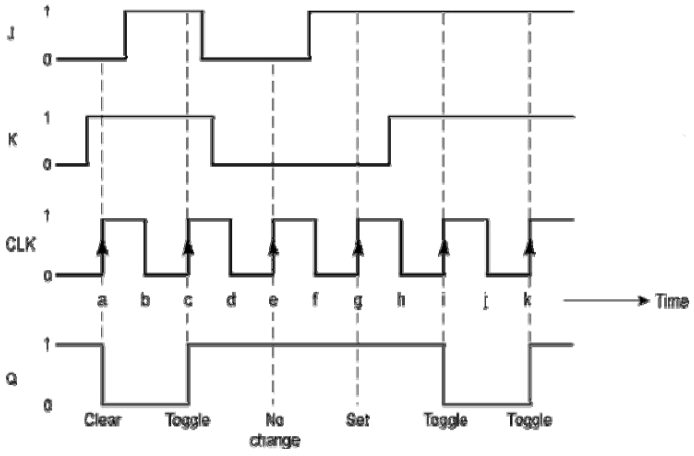
- J=K=1 condition does not result in an ambiguous output



(a)

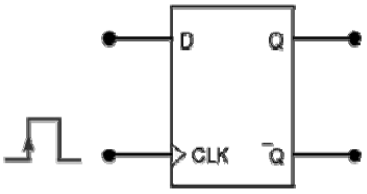
J	K	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	Q_0 (toggles)





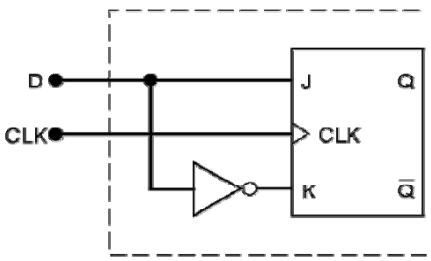
Clocked D Flip-Flop

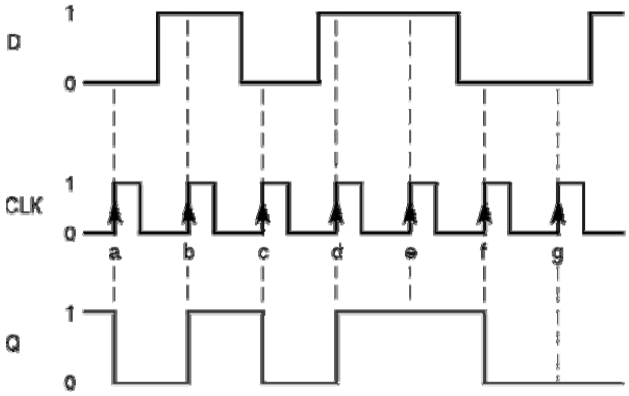
- It can be obtained from J-K Flip-Flop



(a)

D	CLK	Q
0	↑	0
1	↑	1

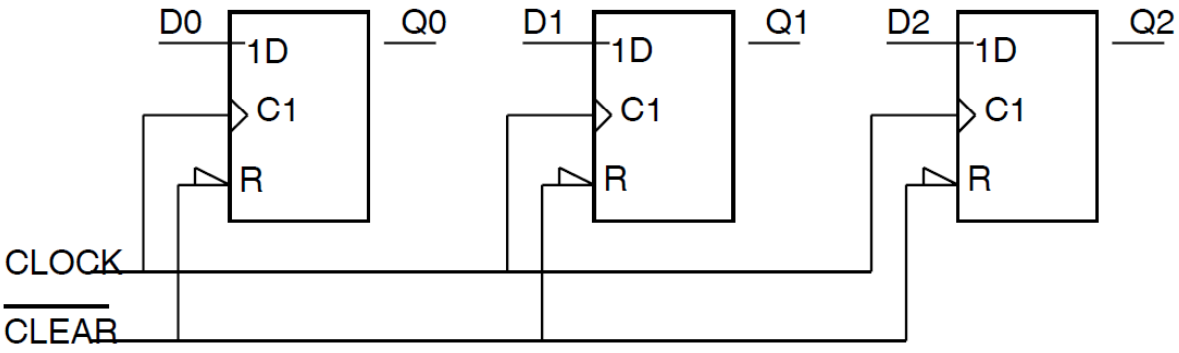




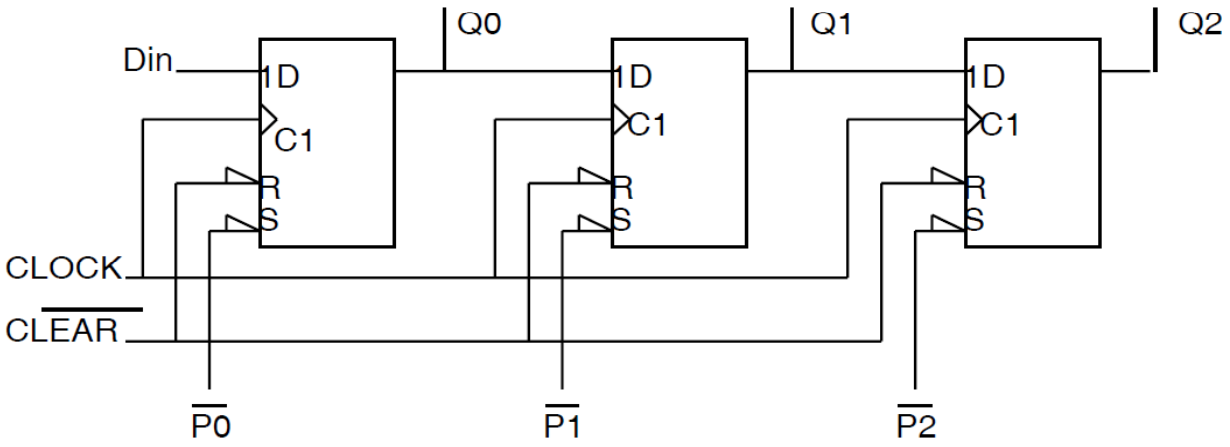
Registers

- A register is a digital electronic device capable of storing several bits of data
  - Normally made from D-type flip-flops with asynchronous RESET inputs
  - Operates on the bits of the data word in parallel
  - Data on each data input is stored in the flip-flop on the rising edge of CLOCK
  - The data can be read from the Q outputs
  - The register can be cleared (zeroed) by asserting the CLEAR inputs

3-bit Parallel in/Parallel out

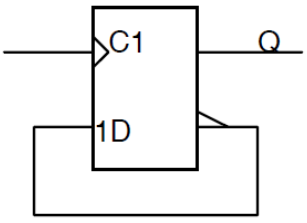


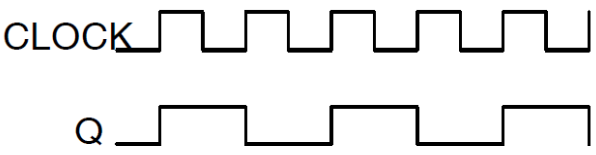
Shift Registers



Divide by 2 Circuit

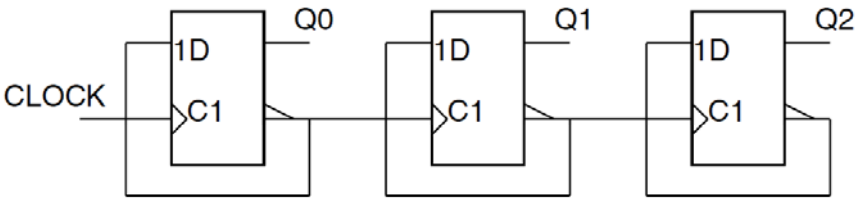
- Consider a D-type flip-flop with Q connected to D

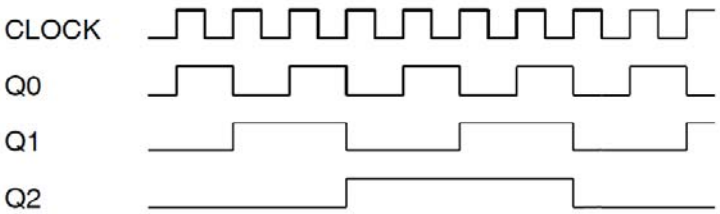




- The frequency of Q is half the frequency of CLOCK

Asynchronous Binary Counters





Decimal	Q2	Q1	Q0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

- Q0 = CLOCK / 2
- Q1 = Q0 / 2
- Q2 = Q1 / 2

Asynchronous Binary Counters

- Limitations
  - Consider the change from count 3 to count 4
    1. CLOCK goes from low to high
    2. Q0 goes from high to low
    3. Q1 goes from high to low
    4. Q2 goes from low to high
  - The "CLOCK-TO-Q" delay of a typical flip-flop is about 30 ns
  - Hence total time needed is about 90 ns.
  - Hence max CLOCK frequency is = 11.1 MHz